

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,320,065 B2
APPLICATION NO. : 09/843178
DATED : January 15, 2008
INVENTOR(S) : Jason Gosior et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 20, delete text beginning at line 2 with "1. A programmable, single-chip" to and including "(5) . . ." at column 20, line 19, and insert therefor:

--1. A programmable, single-chip embedded processor comprising:

(a) a multiple-bit, multithreaded processor core comprising a single processor pipeline having a 'k' number of pipeline stages shared by one or more independent processor threads, the number 'k' being equal to at least four, and a number 'n' of said processor threads being equal to or less than 'k';

(b) an instruction execution logic mechanism engaged with said processor core for executing instructions from a built-in instruction set;

(c) a supervisory control unit, controlled by one or more control threads selected from said processor threads, for examining the processor core state and for controlling the operation of said processor core, said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation;

(d) a memory capable of storing data comprising instructions from said instruction set, said memory being internally integral to the embedded processor, and comprising a main RAM and a boot ROM; and

(e) a peripheral adaptor internally integral to the embedded processor and engaged with said processor core for transmitting input/output signals to and from said processor core;

wherein:

(f) each of the 'n' program threads occupies a unique pipeline stage at any given time;

(g) each program thread advances to the next pipeline stage with every clock cycle;

(h) for a given program thread, the pipeline completes a one-word instruction every 'k' clock cycles;

(i) a first selected program thread is adapted to wait for a specified number of clock cycles for a response from a designated peripheral device; and

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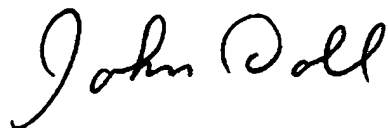
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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(j) a second selected program thread is adapted to re-initialize said first selected program thread if the designated peripheral device does not respond within the specified number of clock cycles.--

Signed and Sealed this

Seventh Day of April, 2009

A handwritten signature in black ink that reads "John Doll". The signature is written in a cursive, flowing style.

JOHN DOLL
Acting Director of the United States Patent and Trademark Office